WHAT IS CLAIMED IS:

1. A shift register comprising:

flip-flops of a plurality of stages to which a clock signal is inputted; and

switching means that is installed in each of the flip-flops of a plurality of stages and that controls the input of the clock signal,

wherein, in response to the output signal of the flip-flop on the i-numbered stage (where i is an arbitrary integer) among the flip-flops of the stages, the switching means on the (i + 1)-numbered stage is controlled so that the input of the clock signal to the flip-flop on the (i + 1)-numbered stage is controlled and an output pulse having the same width as the pulse width of the clock signal is generated.

2. The shift register as defined in claim 1, wherein M($M \geqq 2$)kinds of clock signals are successively inputted to every (M - 1) number of the flip-flops on a plurality of stages.

3. The shift register as defined in claim 2, wherein the M kinds of clock signals are allowed to have such phases that their high-level periods or low-level periods do not overlap each other.

4. The shift register as defined in claim 3, wherein the duty ratio of each of the M kinds of clock signals is preferably set to not more than (100 ×1/M)%.

5. The shift register as defined in claim 2, wherein the flip-flop on each of the stages is a set-reset type flip-flop, and an output pulse of a (i + k × M)-numbered stage (k ≧ 1) is inputted to a reset terminal of a flip-flop on an i-numbered stage.

6. The shift register as defined in claim 2, wherein the flip-flop on each of the stages is a set-reset type flip-flop, and an output signal of a flip-flop on a (i + k × M)-numbered stage (k ≧ 1) of the plural stages is inputted to a reset terminal of a flip-flop on an i-numbered stage.

7. The shift register as defined in claim 1, further comprising:

an input stabilizing section for stabilizing an input to each of the flip-flops on the plural stages which the switching means is opened.

8. The shift register as defined in claim 7, wherein the flip-flop on each of the stages is a set-reset type

flip-flop, and an output pulse of a $(i + k \times M)$-numbered stage ($k \geqq 1$) is inputted to a reset terminal of a flip-flop on an i-numbered stage.

9. The shift register as defined in claim 7, wherein the flip-flop on each of the stages is a set-reset type flip-flop, and an output signal of a flip-flop on a $(i + k \times M)$-numbered stage ($k \geqq 1$) of the plural stages is inputted to a reset terminal of a flip-flop on an i-numbered stage.

10. An image display device comprising:

a display section constituted by a plurality of pixels arranged in a matrix format;

a data signal line driving circuit, connected to a plurality of data signal lines, for supplying to the respective data signal lines image data to be written in the pixels; and

a scanning signal line driving circuit, connected to a plurality of scanning signal lines, for supplying to the scanning signal lines a scanning signal for controlling a writing operation of the image data to the pixels,

wherein the shift register as defined in claim 1 is installed at least in either the data signal line driving circuit or the scanning signal line driving circuit.

11. The image display device as defined in claim 10, wherein at least either the data signal line driving circuit or the scanning signal line driving circuit is formed on a substrate on which the pixels are formed.

12. The image display device as defined in claim 10, wherein a switching element constituting at least either the data signal line driving circuit or the scanning signal line driving circuit is a polycrystal silicon thin-film transistor.

13. The image display device as defined in claim 12, wherein the switching element is formed at a temperature of not more than 600 °C.

14. A shift register comprising:

flip-flops of a plurality of stages that operate in synchronism with clock signals; and

level shifters for voltage-raising the clock signals to be inputted to the flip-flops on a plurality of stages,

wherein: the level shifter is installed in each of the flip-flops on a plurality of stages, and supposing that n is an integer not less than 1, in accordance with the output signal of the flip-flop on the n-numbered stage, a pulse that is voltage-raised with the same width of the pulse width

of the clock signal by the level shifter on a (n + 1)-numbered stage is inputted to the flip-flop on the (n + 1)-numbered stage, and is also outputted as an output signal of the shift register.

15. The shift register as defined in claim 14, wherein each of the level shifter is provided with a current-driving type voltage-raising section.

16. The shift register as defined in claim 15, wherein the output signal of the flip-flop on a n-numbered stage is inputted to the voltage-raising section of the level shifter on a (n + 1)-numbered stage so that the corresponding level shifter is stopped by applying a signal having a level so as to cut off the input switching element.

17. The shift register as defined in claim 15, wherein, the output signal of the flip-flop on a n-numbered stage stops a power supply to the level shifter on a (n + 1)-numbered stage so that the corresponding level shifter is stopped.

18. The shift register as defined in claim 14, wherein the level shifter comprises an output stabilizing means for maintaining an output voltage at a predetermined value at the time of stoppage.

19. The shift register as defined in claim 14, wherein a transistor, which is installed in the level shifter on a (n + 1)-numbered stage and to which a clock signal is inputted, has a gate capacitance that is separated from a transmission line of the clock signal by the output signal of the flip-flop on the n-numbered stage.

20. The shift register as defined in claim 14, wherein, supposing that M is an integer not less than 2, M kinds of clock signals are successively inputted to every M number of the flip-flops on a plurality of stages.

21. The shift register as defined in claim 20, wherein each of the M kinds of clock signals is allowed to have either a phase in which high-level periods do not overlap each other or a phase in which low-level periods do not overlap each other.

22. The shift register as defined in claim 20, wherein the duty ratio of each of the M kinds of clock signals is set to not more than (100 ×1/M)%.

23. The shift register as defined in claim 20, wherein the flip-flop on each of the stages is a set-reset type

flip-flop, and supposing that i and k are integers of not less than 1, an output pulse of a $(i + k \times M)$-numbered stage is inputted to a reset terminal of a flip-flop on an i-numbered stage.

24. The shift register as defined in claim 20, wherein the flip-flop on each of the stages is a set-reset type flip-flop, and supposing that i and k are integers of not less than 1, an output signal of a flip-flop on a $(i + k \times M)$-numbered stage of the plural stages is inputted to a reset terminal of a flip-flop on an i-numbered stage.

25. An image display device comprising:

a display section which includes a plurality of pixels arranged in a matrix format, a plurality of data signal lines placed on the respective columns of the pixels and a plurality of scanning signal lines placed on the respective rows of the pixels and which displays an image on the pixel by a data signal that is sent from the data signal line to each pixel in synchronism with a scanning signal supplied from each scanning signal line so as to form an image;

a scanning signal driving circuit for successively supplying scanning signals having different timing from each other to the scanning signal lines in synchronism with a first clock having a predetermined cycle; and

a data signal line driving circuit for extracting data signals applied onto the respective pixels on the scanning signal line to which the scanning signal has been applied, from a video image signal that has been successively applied in synchronism with a second clock having a predetermined cycle and is representative of a display state of each pixel, and for outputting the resulting data to each of the data signal lines,

wherein at least either the data signal line driving circuit and the scanning signal line driving circuit includes the shift register having the first or second clock signal as a clock signal as defined in claim 14.

26. The image display device as defined in claim 25, wherein at least either the data signal line driving circuit or the scanning signal line driving circuit is formed on a substrate on which the pixels are formed.

27. The image display device as defined in claim 25, wherein the data signal line driving circuit, the scanning signal line driving circuit and the respective pixels include switching elements made of polycrystal silicon thin-film transistors.

28. The image display device as defined in claim 27,

wherein the data signal line driving circuit, the scanning signal line driving circuit and the respective pixels include switching elements that are formed at a temperature of not more than 600 °C.